

B #4
MG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application

Inventor(s): OM P. AGRAWAL et al.

SC/Serial No.: 09/235,615

Filed: January 21, 1999

Title: **FPGA INTEGRATED CIRCUIT HAVING EMBEDDED SRAM MEMORY BLOCKS WITH REGISTERED ADDRESS AND DATA INPUT SECTIONS**



PATENT APPLICATION

) Art Unit: 2819

) Examiner: D. Chang

) Batch No.: V17

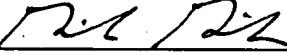
) Notice of Allowance

) Mailing Date: 11/17/00

Customer No. 23910

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Official Draftsman, Commissioner for Patents, Washington, DC 20231**, on February 6, 2001.


Gideon Gimlan, Reg. No. 31,955
Signature Date: February 6, 2001

(Attorney Signature)

SUBMISSION OF FORMAL DRAWINGS TRANSMITTAL LETTER

Official Draftsman
Commissioner for Patents
Washington, DC 20231

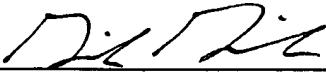
Sir:

Enclosed are 16 sheets of formal drawings for the above-identified patent application.

Subject to the Examiner's approval, please substitute the enclosed drawings for the drawings previously submitted.

Respectfully submitted,

Date: 2-6-2001

By: 

Gideon Gimlan
Reg. No. 31,955
Tel. (408) 748-7300

FLIESLER, DUBB, MEYER & LOVEJOY LLP
Four Embarcadero Center, Suite 400
San Francisco, California 94111-4156
Telephone (415) 362-3800